4.1 A Digitally Modulated Polar CMOS PA with 20MHz Signal BW

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Increased demand for higher data-rate wireless communications has led to the widespread adoption of spectral-efficient signal modulation techniques and communication protocols that encode data in both the amplitude and phase of the RF signal, thereby requiring the use of linear power amplifiers (PAs). The linearity required for such amplifiers is typically achieved by operating them below their maximum output power, at the cost of reduced power efficiency and battery life. Polar transmitter architectures can be used to address the deficiencies of CMOS technology and overcome the conventional trade-off between linearity and efficiency [1]. However, to date no polar transmitter has been reported that meets the signal bandwidth and linearity requirements for IEEE 802.11g 64QAM OFDM signals. The CMOS polar amplifier in this work achieves the linearity and bandwidth required for such signals by employing an array of efficient constant-envelope amplifiers that are digitally modulated to construct the RF output signal. An experimental prototype, implemented in a 0.18μm CMOS technology, operates with a 20MHz signal bandwidth at 1.6GHz and achieves 7.2% power-added-efficiency (PAE) with an EVM of –26.8dB while delivering 13.6dBm linear output power.

Figure 4.1.1 shows the proposed amplification system. The baseband in-phase (I) and quadrature (Q) signals are decomposed into envelope and phase components. The envelope is encoded into a 6b digital code, and the phase is converted into a constant-envelope RF signal that drives an array of parallel current-mode unit amplifiers. The unit amplifiers are digitally activated by the envelope code, and their output currents are combined to shape the RF output. In effect, this system provides a digital-to-analog conversion of the envelope while performing efficient constant-envelope amplification in the RF phase domain.

In ideal class-A PAs, efficiency and output power have a linear relationship, which results in a poor average power efficiency when amplifying signals with a large peak-to-average-power ratio (PAPR). For example, when amplifying an OFDM signal with 10dB PAPR, an ideal class-A amplifier has a maximum average efficiency of 5%. However, since the output current of the polar system proposed in this work is a linear function of the envelope signal, the power efficiency is proportional to the square root of the output power, resulting in 14% average efficiency when amplifying the same OFDM signal.

System simulations indicate that the EVM and the spectral mask specifications for a 64QAM OFDM IEEE 802.11g signal require the use of at least 6 bits in the digital representation of the envelope signal. Thus, the polar PA in this work comprises 64 nominally identical unit amplifiers. As shown in Fig. 4.1.2, each unit amplifier includes a cascode transistor that acts as a switch. The cascode transistor is implemented using a thick-oxide structure in order to accommodate the large output swing. A driver stage is used to provide sufficient voltage drive for the output amplifiers. In the actual implementation, both the unit amplifier and the driver stage are fully differential, and off-chip baluns are used at both the RF input and output.

The digitally modulated polar RF amplifier is essentially a digital-to-RF power converter. Spectral images resulting from discrete-time to continuous-time conversion can violate the spectral mask and the constraints on out-of-band emissions. These could be suppressed by increasing the sampling frequency and interpolating the input or filtering the output of the amplifier. However, in this work, 4× oversampling is combined with 4-fold linear interpolation at the output [2]. Each of the unit amplifiers in the output stage is divided into four parallel sections that are switched sequentially by 4 quadrature-phased clocks.

A micrograph of the polar PA is shown in Fig. 4.1.3. The chip was fabricated in a 0.18μm CMOS technology, and its total area is $1.3\times1.4mm^2$. The placement of the four sections of unit amplifiers, as well as the placement of the unit amplifiers themselves within those sections, follows a common-centroid layout. This layout improves the linearity through spatial averaging and also results in a more uniform distribution of the temperature over the die. The output pads of the amplifier are placed in the center of the output stage to preserve symmetry among the four sections and minimize resistive losses in the output path. Multiple ground pads are positioned symmetrically around the output stage to provide a low impedance path to ground. The chip is directly mounted on a gold-plated PCB to avoid package parasitics.

Figure 4.1.4 shows the system that was used to demonstrate the performance of the polar PA. An IEEE 802.11g 64QAM baseband signal is digitally decomposed into its phase and envelope and loaded into an FPGA. A dual-channel DAC and a quadrature RF modulator convert the digital FPGA output to an analog signal and transform the digital phase to the desired RF phase signal. The FGPA also directly drives the digital envelope input of the prototype PA. The delay mismatch between the two paths is compensated for by delaying the envelope signal digitally and also by adjusting the delay between the reference and quadrature clocks. Figure 4.1.5 shows the measured output spectrum, which meets the spectral mask of the IEEE 802.11g signal. The measured EVM of this 64QAM OFDM signal is –26.8dB. Since no provision for frequency tuning is included in the experimental prototype, its center frequency of 1.6GHz is less than the targeted 2.4GHz. This discrepancy can be attributed to uncertainty in the models for the passive components.

The suppression of the out-of-band spectral images by 4-fold linear interpolation is illustrated in Fig. 4.1.6. The 64QAM OFDM output power (including 1.1dB loss in the output balun) is 13.6dBm with an average PAE of 7.2%. The measured input power is 2dBm. The prototype PA can be converted into a linear amplifier by setting all the envelope bits to one and driving the RF phase input of the PA with a linear RF OFDM signal. The measured PAE of the amplifier in this linear mode is 3.1%, confirming that the digital modulation architecture more than doubles the measured power efficiency. Figure 4.1.7 summarizes the measured performance.

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References:
[1] R. B. Staszewski, *et. al.*, "All-Digital PLL and Transmitter for Mobile Phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469-2482, Dec., 2005.
[2] Y. Zhou and J. Yuan, "A 10-Bit Wide-Band CMOS Direct Digital RF Amplitude Modulator,", *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1182-1188, July, 2003.

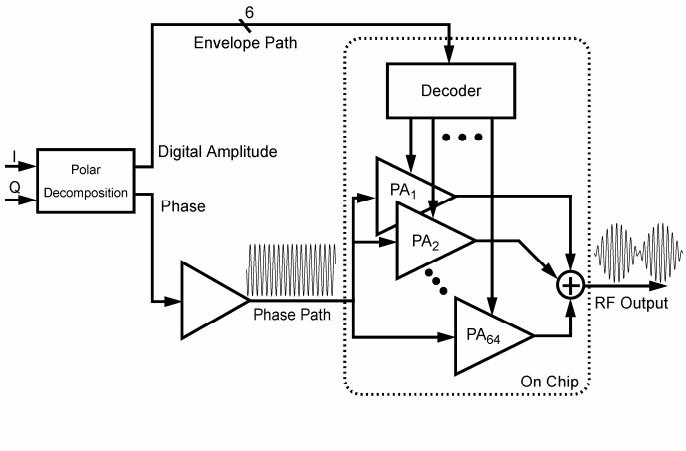

Figure 4.1.1: RF digital polar PA architecture.

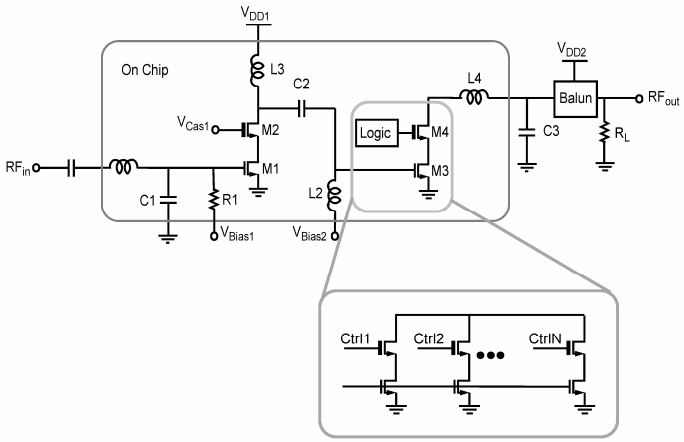

Figure 4.1.2: PA schematic (single-ended representation).

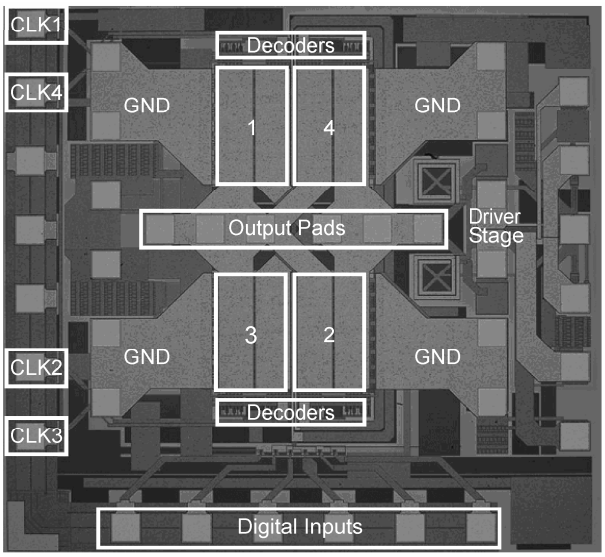

Figure 4.1.3: Die micrograph.

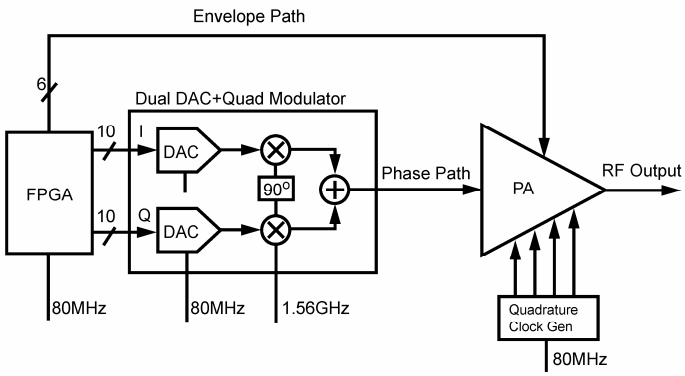

Figure 4.1.4: Demonstration system.

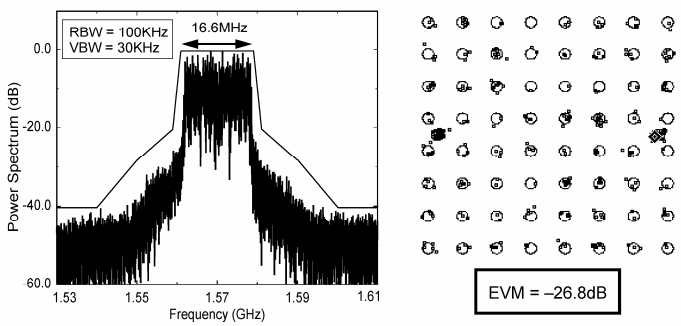

Figure 4.1.5: Measured OFDM output spectrum and constellation.

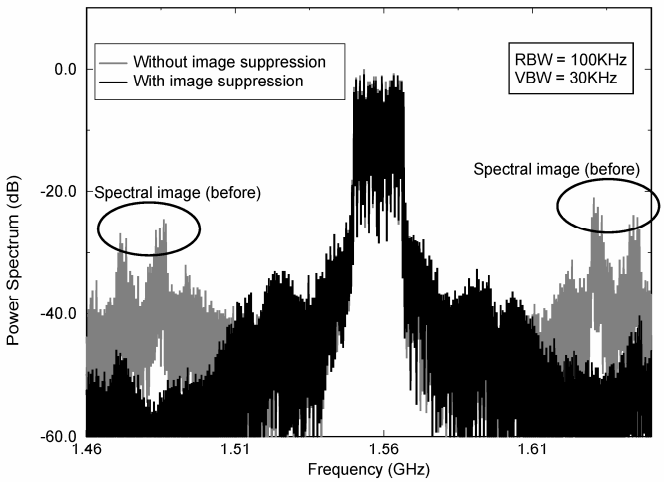

Figure 4.1.6: Output spectrum with and without L-fold linear interpolation.

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Technology	0.18μm CMOS, 2P5M
Supply Voltage Digital Hardware Driver Stage Output Stage	 1.8V 2.2V 1.7V
Linear 64 QAM OFDM Output Power	13.6dBm
EVM for 64 QAM OFDM	–26.8dB
Dissipated Power Output Stage Driver Stage Digital	 247mW 66mW 3.4mW
PAE (for 64QAM OFDM)	7.2%
Center Frequency	1.56GHz
Total Chip Area	1.8mm^2

Figure 4.1.7: Performance summary.

